IN THE FIGURES

A replacement sheet is included for Figure 3. In this replacement sheet, the element number for multiplexer 350 was changed to 330 because this element number was already used for VSS.

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REMARKS

Applicants respectfully request reconsideration of the pending claims. In that regard, consider the title of the present application, which refers to a "delay-matched ASIC conversion" of a programmable logic device (PLD). As discussed in the background section of the specification, a user's design for a programmable logic device is typically optimized for the associated propagation delays in the PLD's routing structure. Despite the lower cost of ASIC conversions, a user will thus often be reluctant to attempt such a conversion because of the uncertainty of matching propagation delays.

Applicants have provided a delay-matched ASIC conversion such that users may now take advantage of the lower costs of ASIC conversion. The delay matching may be implemented using a number of different embodiments. For example, as discussed with respect to PLD routing structure multiplexer 530 shown in Figure 5, the selection of one input such as trace 531 adds loading on unselected inputs (such as bus VX2) that affects propagation delays. To model this loading in an ASIC conversion and hence be delay-matched to the corresponding PLD, a programmable diode load (element 640) may be used as discussed with respect to Figure 6.

Another factor affecting propagation speed in a PLD routing structure is the channel sizes for the transistors used to construct the buffers (should the routing structure be buffered). These channel sizes depend upon the particular manufacturing process being used to produce the PLD. Even for the same PLD within a manufacturer's product lineup, these process variations may produce devices ranging from those with relatively fast propagation speeds to those with relatively low propagation speeds. To model these process variations, programmable buffers such as buffer 700 may be used in the ASIC conversion. Depending

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upon the control signals as selected by a mask programming step, buffer 700 provides the appropriate propagation delay.

Claim 1 has been amended to emphasize the delay-matched nature of the ASIC conversion provided by the Applicants. In particular, claim 1 now recites the limitation of "wherein the ASIC routing structure is adapted to be delay matched to propagation delays in the PLD routing structure." The cited prior art stands in sharp contrast to the advantageous ASIC conversion recited in claim 1. For example, the Lien reference (USP 6,211,697) as suggested by the title is directed to an integrated circuit that includes both an FPGA and a "hard gate array." As discussed in the background section of this patent, such a mixed device complicates configuration because different software must be used to program the FPGA vs. that used to design the hard gate array. To allow the use of the same software, Lien designed the hard gate array to have the same underlying logic and routing structure as discussed, for example, with respect to Figures 3 and 4. However, note that the hard gate array is not an ASIC conversion of the programmed FPGA. Instead, it is merely structure that may be designed using the same software. Using this software, a user of the Lien device configures the FPGA to perform one task and the hard gate array to do something entirely different. The hard gate array is not a replacement for the FPGA – it cannot possibly be used as such because the two devices are integrated into the same integrated circuit.

In sharp contrast, the ASIC conversion recited in claim 1 is directed to a conversion of a programmed FPGA whose routing structure will have a certain propagation delay depending upon its configuration. It is not simply directed to the replication of the underlying structure of the FPGA as in Lien. Thus, claim 1 recites the limitation of "wherein the ASIC routing structure is adapted to be delay matched to propagation delays in the PLD routing structure." As discussed above, these delays will depend upon the programming used to configure the FPGA. Because Lien makes no teaching or suggestion for the ASIC conversion of a

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configured FPGA, the routing delays are of no concern in Lien – indeed, Lien makes no mention whatsoever regarding the matching of routing delays.

Applicant notes that the section in Lien cited to allegedly provide such a delay matching (Col. 12, lines 39+, 51+) explicitly teaches away from any delay matching: what Col. 12, lines 30 – 49 describes is the interfacing between Lien's FPGA and hard gate array. Because the hard gate array operates faster, results from the hard gate array must be delayed in flip-flops 264, etc., of Figure 12 before the FPGA would be ready to receive the data. Similarly, lines 49 – 67 in Col. 12 describes an alternate use of JTAG scan cells to provide this delay of hard gate array results. Such delay (whether occurring in flip-flops or scan cells) has nothing to due with providing a teaching or suggestion that routing delays in the hard gate array are matched to the corresponding PLD routing delays. Accordingly, claim 1 and its dependent claims 2 – 13 are allowable over the Lien reference.

Applicants gratefully acknowledge the indication that claims 10 through 13 contain allowable subject matter. Claims 10 and 11 have been amended in light of the amendment to claim 1 to provide specific instances of how the delay matching adaptation recited in claim 1 may be implemented. The objection to claim 10 has also been addressed.

Claim 17 has been amended analogously as discussed with respect to claim 1. Accordingly, claims 17 and its dependent claims 18 – 20 are allowable over the Lien reference.

Claim 32 recites the limitation of "the ASIC routing structure adapted to produce a signal propagation delay that matches substantially the signal propagation delay in the corresponding PLD programmable routing structure." As discussed above, Lien provides no teaching or suggestion for such an advantageous limitation. Accordingly, claims 32 and its dependent claims 33 – 37 are allowable over the Lien reference.

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In addition, some minor typographical errors in the specification and drawings have been corrected.

CONCLUSION

Accordingly, Applicants respectfully submit that Claims 1 – 13, 17 – 20, and 32 – 37 are in proper form for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is solicited.

If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the Commissioner for Patents, Fax No. 703-872-9306 on the date stated below.

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